REMARKS

Applicant appreciates the courtesy extended by the Examiner during the interview of June 9, 2005. The independent claims were discussed in view of the art of record. No formal agreement was reached. Applicant's position taken during the interview is included in the Remarks herein.

This paper is responsive to the Non-Final Office Action dated March 15, 2005. Claims 1-7, 9-27 and 31-33 were pending. Claims 23, 26-27 and 32-33 stand rejected under 35 U.S.C. § 112, first paragraph. Claims 1-7 and 13-20 stand rejected under 35 U.S.C. § 112, second paragraph. Claims 1-7, 9, 14-15, 17, 19-20, 26, and 31-32 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Baweja (US 6,212,599 B1). Claims 10-13, 16, 18, and 21-25 stand rejected under 35 U.S.C. § 103 as being unpatentable over Baweja in view of AMBA Interconnection Schemes, Application Note 05, ARM DA 0005A, 1993 (hereinafter AMBA). By way of the present amendment claims 15, 22, 23 and 25 have been canceled.

Rejection under 35 U.S.C. § 112, second paragraph

While applicant believes that the term "independent" is clear and that the term can be found in numerous claims in issued patents, applicant has removed the term "independent" from claims 1 and 14. Accordingly, applicant respectfully requests that the rejection under 35 U.S.C. § 112, second paragraph be reconsidered and withdrawn.

Rejection Under 35 U.S.C. § 112, first paragraph

The rejection of claim 23 under 35 U.S.C. § 112, first paragraph is moot in view of its cancellation.

Claim 26 has been amended to remove the language "in the integrated circuit". Accordingly, applicant respectfully requests that the rejection of claim 26 under 35 U.S.C. § 112, first paragraph be reconsidered and withdrawn.

With respect to claim 32, the applicant respectfully submits that applicant's disclosure fully supports the claim as recited. Applicant notes that Fig. 7 shows a region 705 of integrated

circuit 702 that remains powered when region 703 is shut off. That region 705 includes logic 707. Logic 707 receives an externally supplied reset signal that causes logic 707 to output an appropriate self refresh control signal. Claim 31 (on which claim 32 depends) recites a second circuit (e.g., logic 707) coupled to cause the memory control signal to be at a logic level to maintain a memory in a self refresh state, and that during a power savings state in which power to the memory control circuit (e.g., memory controller 704) is turned off, a reset signal coupled to the second circuit, when asserted, causes the second circuit to keep the memory control signal at the logic level to maintain the memory in a self refresh state. Claim 32 recites that second circuit (e.g., logic 707) and the memory control circuit (e.g., memory controller 704) are on the same integrated circuit. That is exactly what is shown in Fig. 7 and described in the accompanying description. Accordingly, applicant respectfully requests that the rejection of claim 32 under 35 U.S.C. § 112, first paragraph be reconsidered and withdrawn.

Rejection under 35 U.S.C. § 102(e) over Baweja

Claim 1

Amended claim 1 recites supplying at least one memory control signal to the memory from a first integrated circuit in the computer system during an operational state; and supplying the memory control signal from another location in the computer system when the computer system is in a power savings state to maintain memory in the self refresh state. In contrast Baweja teaches in Fig. 2 that CKE signal 260 is supplied from suspend memory controller 220 in all states both operational and power savings. In Fig. 3, the CKE signal is shown to be formed by ANDing the SCKE signal from the state machine 310 in the suspend well 220 with the SDCKE 240 from the first memory controller 210 in AND logic 320. Col. 5, lines 16-18. Baweja also teaches that the suspend memory controller 220 acts as part of the memory system controller 200 during normal operation. Col. 4, lines 32-34. Applicant respectfully submits that Figs. 2 and 3 of Baweja makes clear that the SDCKE signal 240 is not supplied to the memory SDRAM 225, nor is the SCKE signal supplied to the memory.

Claim 1 requires that the memory control signal be supplied from another location in the power savings state. In Baweja the memory control signal is always supplied from AND logic

320. Thus, applicant respectfully requests that the rejection of claim 1 and all claims dependent thereon be reconsidered and withdrawn.

Claim 9

With respect to claim 9, the claim recites controlling at least one memory control signal being supplied to the memory from a first integrated circuit according to an operational state. The claim further recites controlling the memory control signal from another location in a power savings mode. The claim further recites disabling a switch coupling the memory control signal from the first integrated circuit to the memory by driving a switch enable signal from the other location. Baweja fails to teach driving a switch enable signal to disable the switch and isolating the first integrated circuit from the memory during the power savings state.

The Office action relies on AND gate 320 as the switch and the SCKE signal as the switch enable signal. However, if the SCKE signal is the switch enable signal then it is not clear how the memory control signal is supplied from another location in the power savings state. Baweja teaches that CKE signal 330 is supplied from the same location (AND gate 320) regardless of whether Baweja is in a power savings state or an operational state. SDCKE 240 is supplied from the first memory controller 210 in normal operational mode and SCKE from state machine 310 in power savings mode. Assuming *arguendo* that SCKE signal does correspond to the switch enable signal, applicant notes that paragraph 8 of the Office action identifies 310 as the other location supplying the memory control signal and thus the memory control signal is the SCKE signal. The SCKE signal cannot be both the switch enable and the memory control signal. Accordingly, applicant respectfully submits that claim 9 and all claims dependent thereon distinguish over Baweja.

Claim 14

Claim 14 has been amended to include claim 15. Amended claim 14 recites a first integrated circuit including a memory control circuit coupled to the system memory to supply the at least one memory control signal during an operational state; and a second integrated circuit coupled to supply the memory control signal at the first value (for self refresh) during a power savings state. Amended claim 14 further recites an isolation circuit external to the first and

second integrated circuit as shown in the embodiment in Fig. 5. Baweja fails to teach that isolation circuit. Baweja teaches in Fig. 2 that CKE signal 260 is supplied from suspend memory controller 220 in all states both operational and power savings. In Fig. 3, the CKE signal is shown to be formed by ANDing the SCKE signal from the state machine 310 in the suspend well 220 and by SDCKE 240 from the first memory controller 210. Further, claim 14 requires that the memory control signal be supplied from a first integrated circuit during an operational mode and from a second integrated circuit during a power savings mode. Baweja does not teach that. Accordingly, applicants respectfully request that the rejection of claim 14 and all claims dependent thereon be reconsidered and withdrawn.

Claims 26 and 31

Amended claim 26 recites that an asserted reset signal holds the memory control signal at the first value in the first integrated circuit during the power savings state. Fig. 7 illustrates such an embodiment. Although Applicant respectfully disagrees with the position stated in the Office Action that the limitation of the asserted reset signal is met by the SCKE signal, applicant has amended claim 26 to recite that the reset signal initializes the first region to supply the memory control signal at the first value after the power savings state. Support for the amendment can be found on page 17, line 30 to page 18, line 4. Applicant respectfully points out that there is no teaching in Baweja that the SCKE is a reset signal or that the reset signal initializes the first region. Applicant points out that Baweja teaches reset signals (e.g., PCIRST# and CPURST#) but fails to teach either that the SCKE is a reset signal or that any of the reset signals discussed are utilized to hold the memory control signal at the first value in the first integrated circuit during the power savings state. Applicant points out that Baweja teaches in Fig. 4, that the reset signals PCIRST# and CPURST# are not even asserted while main power is off. Thus, those resets can not be used as claimed to hold the memory control signal at the first value (self refresh state) during the power savings state. Instead, Baweja teaches that the resets are used to reset the registers. Col. 6, lines 34-35. Thus, applicant respectfully submits that claim 26 and all claims dependent thereon distinguish over Baweja and the other references of record.

With respect to amended claim 31, applicant respectfully submits that Baweja fails to teach , a reset signal that, when asserted, causes the second circuit to keep the memory control

signal at the logic level to maintain the memory in a self refresh state. Claim 31 has been amended to recite that the memory control circuit is initialized by the asserted reset signal to supply the memory control signal at the logic level to maintain the memory in a self refresh state after power to the memory control circuit is turned on following the power savings state. Applicant submits there is no such teaching associated with the SCKE signal that the Office Action maintains is a reset signal. Thus, applicant respectfully submits that claim 31 and all claims dependent thereon distinguish over Baweja and the other references of record.

Rejection under 35 U.S.C. § 103(a)

Claim 16 recites that the second integrated circuit is coupled to provide a high impedance on an output terminal, during an operational state of the computer system, the output terminal being coupled to the isolation circuit and the memory to provide the memory control signal, and wherein the second integrated circuit is coupled to drive the output terminal and thereby the memory control signal to a low voltage level during the power savings state. The Office Action states that it would have been obvious to combine Baweja and AMBA because tristate drivers of AMBA allow multiple connections while preventing the requirement for external gates and switches. Applicants submit that this teaches against claim 16 since amended claim 14 (on which claim 16 depends) explicitly recites an external switch. Applicant respectfully submits that Baweja and AMBA, even when combined, fail to teach the isolation circuit and use of high impedance as recited in claim 16.

Claim 21 has been amended and recites isolation means to isolate the first means from the system memory during the power savings state. Applicant submits that the structure corresponding to this claim is shown in Fig. 5 and includes switch 224. Applicant submits that neither Baweja nor AMBA teach that structure or it equivalent.

Amended claim 24 recites an integrated circuit with a first and second output terminal. The first output terminal supplies a memory control signal to a memory that is held at a first logic level to keep the memory in a self refresh state, the integrated circuit responsive to a first operational state of the computer system to place the output terminal at a high impedance level and responsive to a power savings state in the computer system to supply the first logic level on the output terminal. The second output terminal supplies a control signal for a switch external to

the integrated circuit. The integrated circuit is responsive to the first operational state of the computer system to place the second output terminal at a logic level causing the switch to pass through an operational memory control signal coupled to an input of the switch as the memory control signal in the first operational state and responsive to the power savings state to supply a different logic level at the output terminal, the second logic level causing the switch to not pass through the operational memory control signal.

Applicant respectfully submits that Baweja, alone or in combination with AMBA fails to teach an integrated circuit having the first and second output terminals of claim 24. The Office Action states that it would have been obvious to combine Baweja and AMBA because tristate drivers of AMBA allow multiple connections while preventing the requirement for external gates and switches. Applicants submit that this teaches against claim 24 since amended claim explicitly recites an external switch. Applicant respectfully submits that Baweja and AMBA, even when combined, fail to teach amended claim 24.

In summary, claims 1-7, 9-14, 16-21, 24, 26-27 and 31-33 are in the case. All claims are believed to be allowable over the art of record, and a Notice of Allowance to that effect is respectfully solicited. Nonetheless, if any issues remain that could be more efficiently handled by telephone, the Examiner is requested to call the undersigned at the number listed below.

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Respectfully submitted,

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